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Application 09/871383(20020089000-A1).
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H01L 29/06
H01L 29/70

# BIDIRECTIONAL BIPOLAR STATIC INDUCTION DEVICE

I had sent reply No.4 to USPTO on 10.03.2003.

According to the status, USPTO had sent me a letter on 10.16.2003 but I have not received it.

I ask to cancel examination of devices without thick channels, because the latch current of such devices equals zero or is close to zero. Unfortunately, the boundary between these devices is not indicated in the application clearly.

"paragraph 0001". The invention relates to microelectronics and more particularly to bipolar static induction devices -- transistor and transistor-thyristor (transistor, which can be latched) with elements of a control circuit. Any device, according to the present invention can be latched. However, if a thick channel drain electrode have been connected to an ordinary channel drain electrode and if the latch current of the device exceeds the maximum current, such device can be considered as the device without latching, i.e. the transistor.

## background of the invention

"between paragraph 0001 and 0002". There exists a static induction type semiconductor device is used as a power transistor. It is of the surface gate type and is used for providing a high current density. The static induction type semiconductor device provides a plurality of a small source regions surrounded by a gate region. According to this structure the channel region beneath the source region becomes small, thereby increasing the stored carrier density and enabling a large main current to flow when using a small gate current, thereby achieving a high current amplification ratio. A thin insulating film provided on the surface of the n+-source region operates as a tunnel-oxidized film, thereby enabling electrons to be injected into the source region but preventing the positive holes from being drawn out. Therefore, as the consumption of positive holes store in the channel region decreases, a sufficiently large source current is allowed to flow even if a further smaller gate current is injected, thereby further increasing the current amplification factor[1]. The drawbacks of the transistor are that it cannot operate on circuits of alternating voltage and that the current density is insufficient.

There exists a vertical JFET, in which a gate and a channel are formed by the implantation of an impurity in a doped epitaxial layer through mask - a doped polysilicon drain electrode[2]. The method provides forming of the transistor with channel thickness equal about 10.sup.-7 m. The drawback of the transistor is that it cannot operate on alternating voltage circuits.